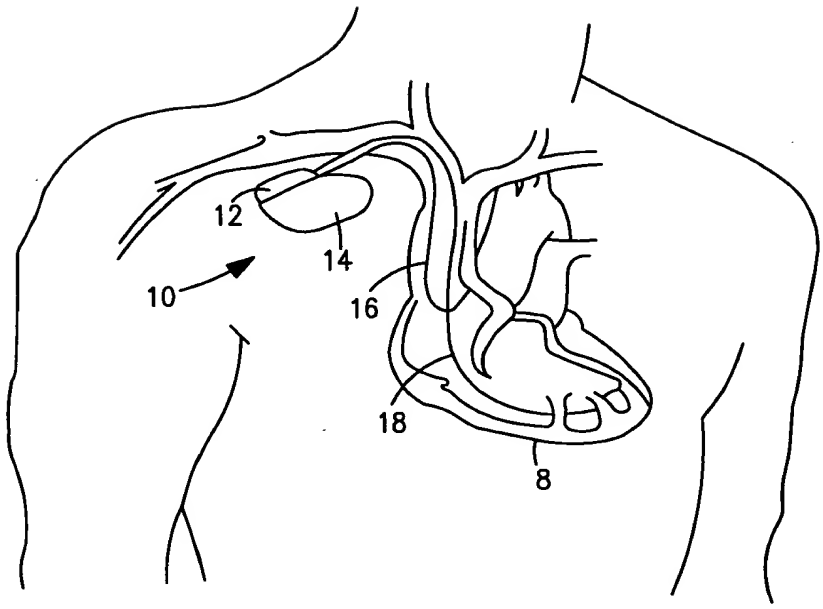

FIG. 1

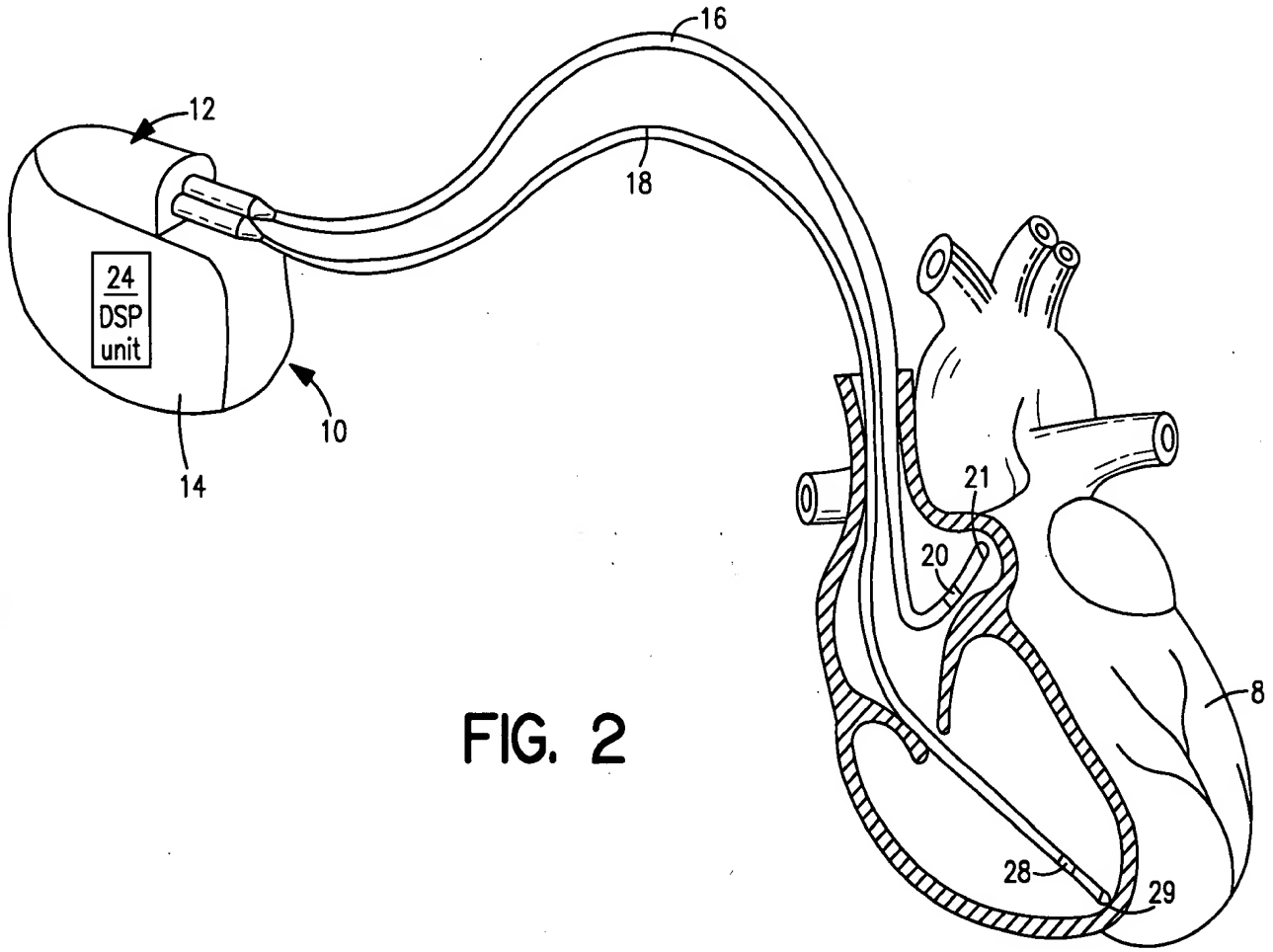

FIG. 2

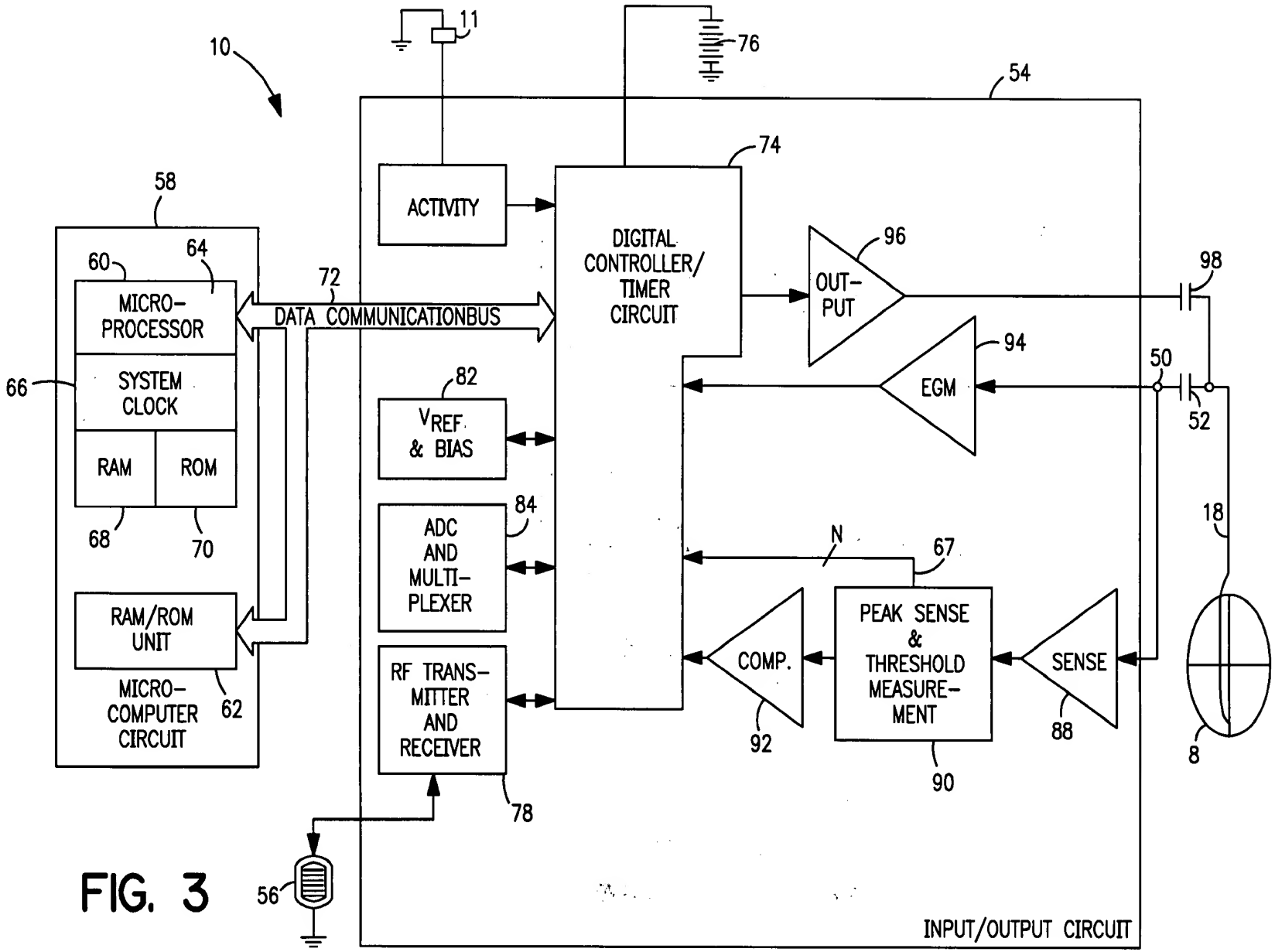

FIG. 3

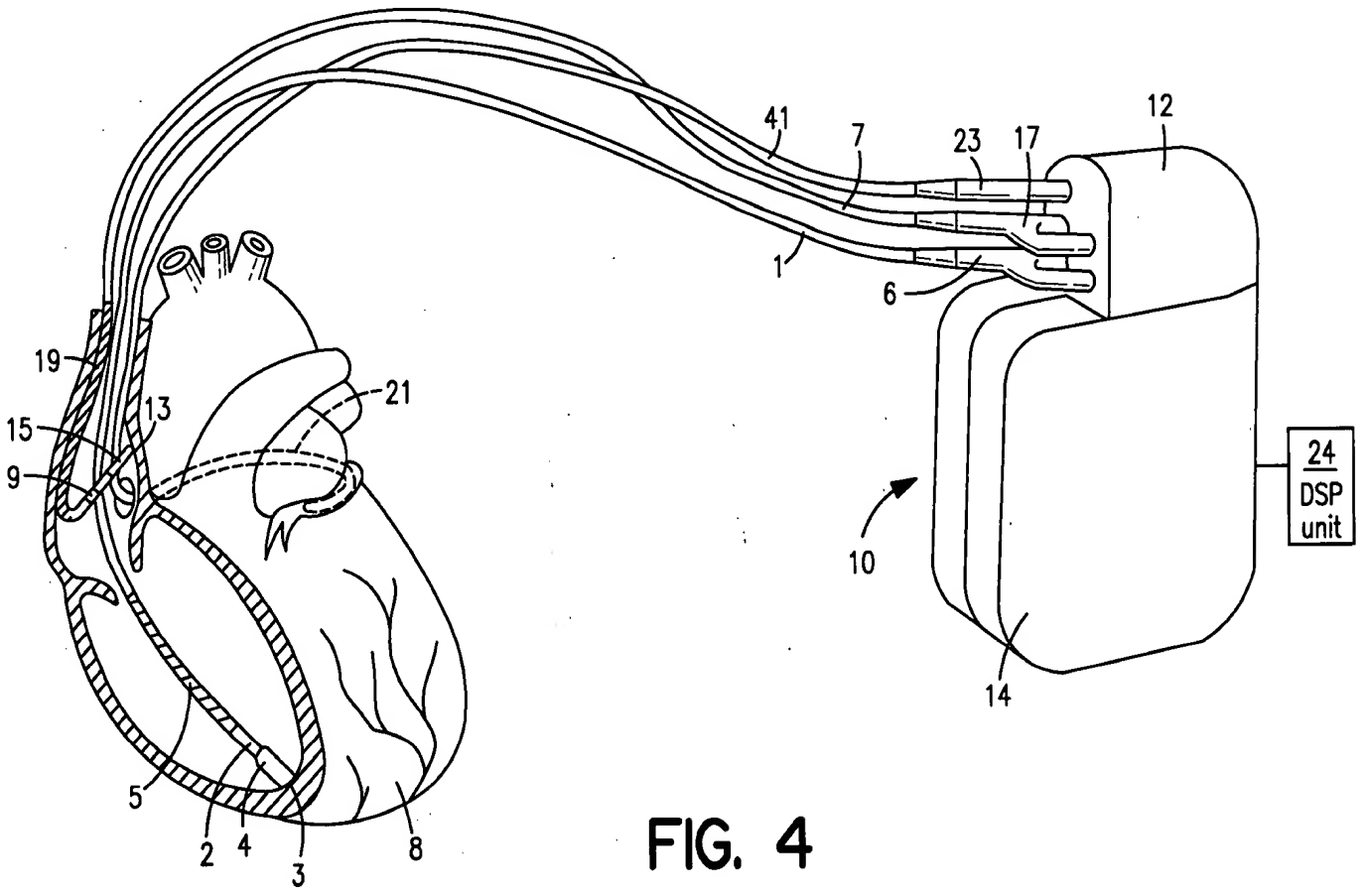

FIG. 4

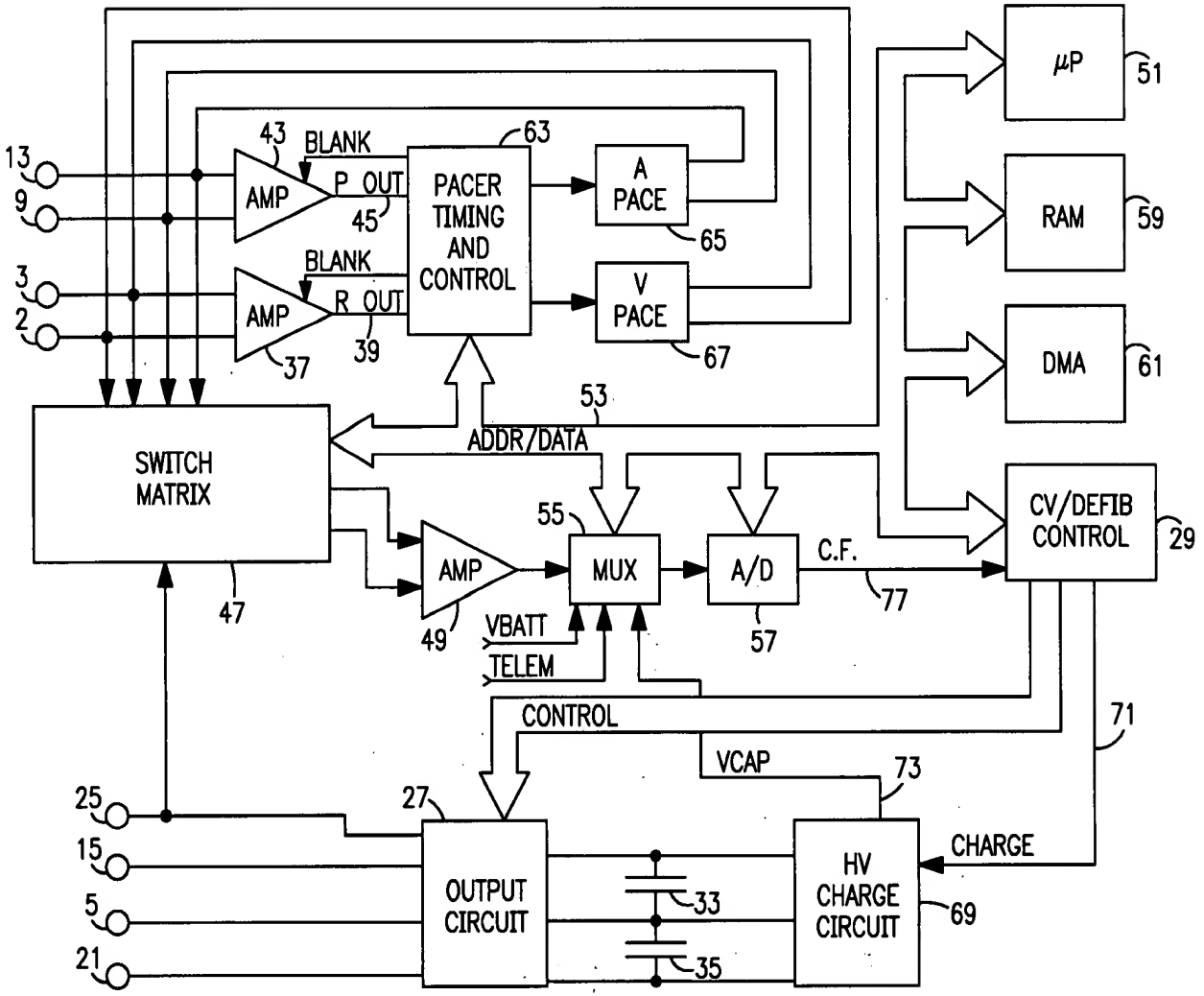
μP
51
RAM
59
DMA
61
CV/DEFIB CONTROL
29
PACER TIMING AND CONTROL
63
A PACE
65
V PACE
67
AMP
43
BLANK
P OUT
45
AMP
BLANK
R OUT
39
37
13
9
3
2
SWITCH MATRIX
47
53
ADDR/DATA
AMP
49
55
MUX
A/D
57
C.F.
77
VBATT
TELEM
CONTROL
71
VCAP
73
25
15
5
21
27
OUTPUT CIRCUIT
33
35
HV CHARGE CIRCUIT
69
CHARGE

FIG. 5

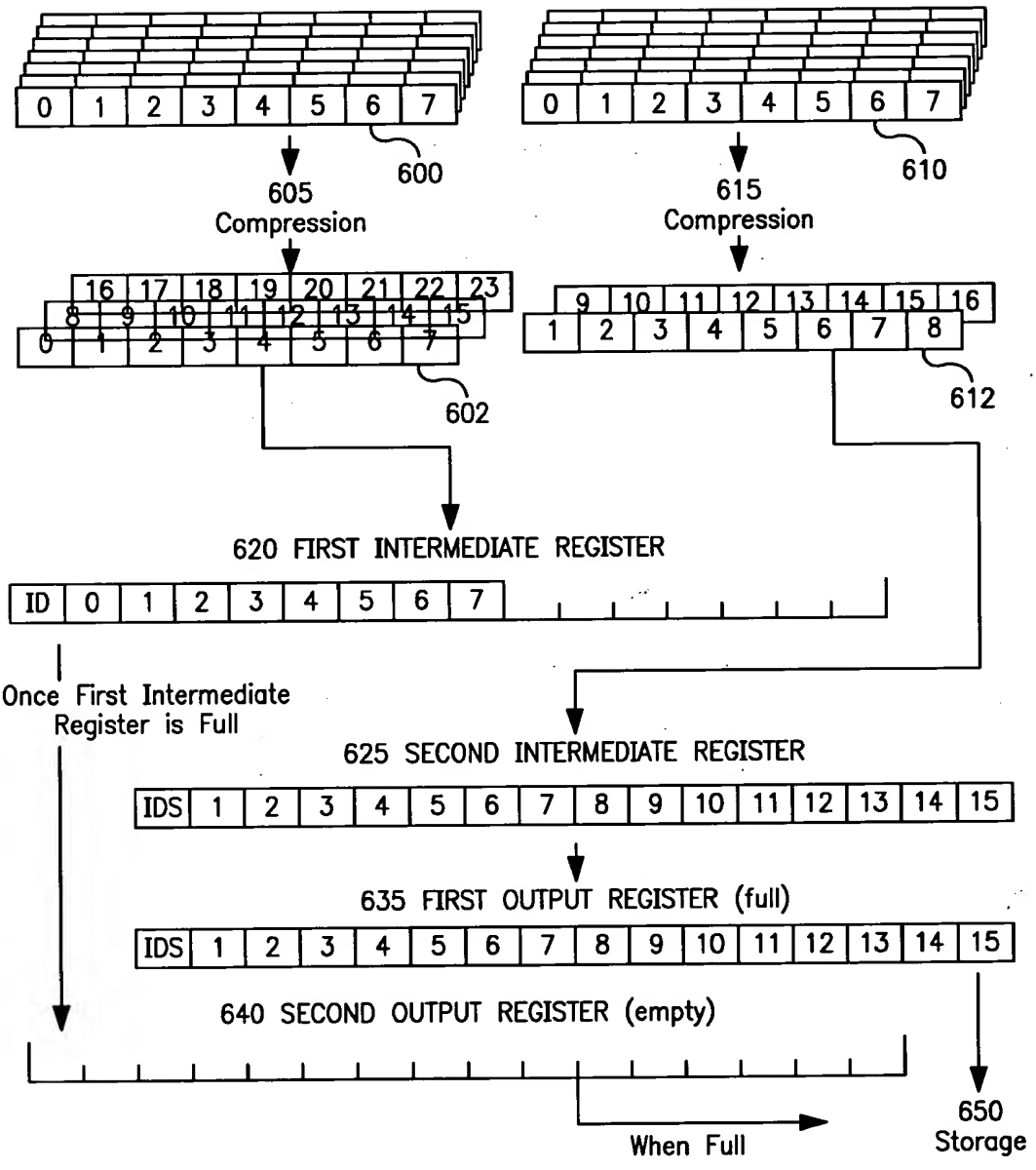
0 1 2 3 4 5 6 7
600
605
Compression
0 1 2 3 4 5 6 7
610
615
Compression
16 17 18 19 20 21 22 23
8 9 10 11 12 13 14 15
0 1 2 3 4 5 6 7
602
9 10 11 12 13 14 15 16
1 2 3 4 5 6 7 8
612
620 FIRST INTERMEDIATE REGISTER
ID 0 1 2 3 4 5 6 7
Once First Intermediate Register is Full
625 SECOND INTERMEDIATE REGISTER
IDS 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
635 FIRST OUTPUT REGISTER (full)
IDS 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
640 SECOND OUTPUT REGISTER (empty)
When Full
650
Storage

FIG. 6

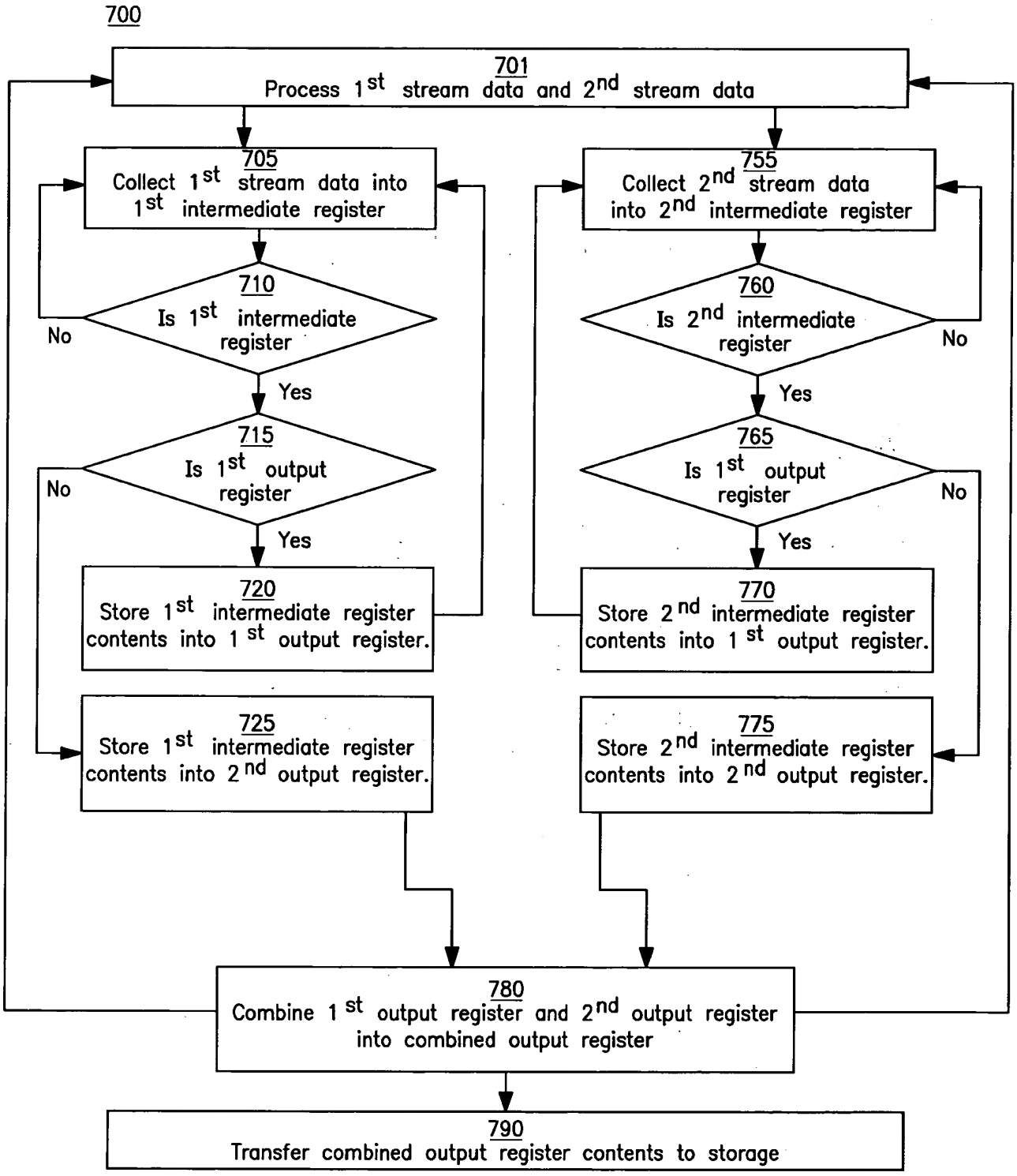
700
701
Process 1st stream data and 2nd stream data
705
Collect 1st stream data into 1st intermediate register
710
Is 1st intermediate register
No
Yes
715
Is 1st output register
No
Yes
720
Store 1st intermediate register contents into 1st output register.
725
Store 1st intermediate register contents into 2nd output register.
755
Collect 2nd stream data into 2nd intermediate register
760
Is 2nd intermediate register
No
Yes
765
Is 1st output register
No
Yes
770
Store 2nd intermediate register contents into 1st output register.
775
Store 2nd intermediate register contents into 2nd output register.
780
Combine 1st output register and 2nd output register into combined output register
790
Transfer combined output register contents to storage

FIG. 7

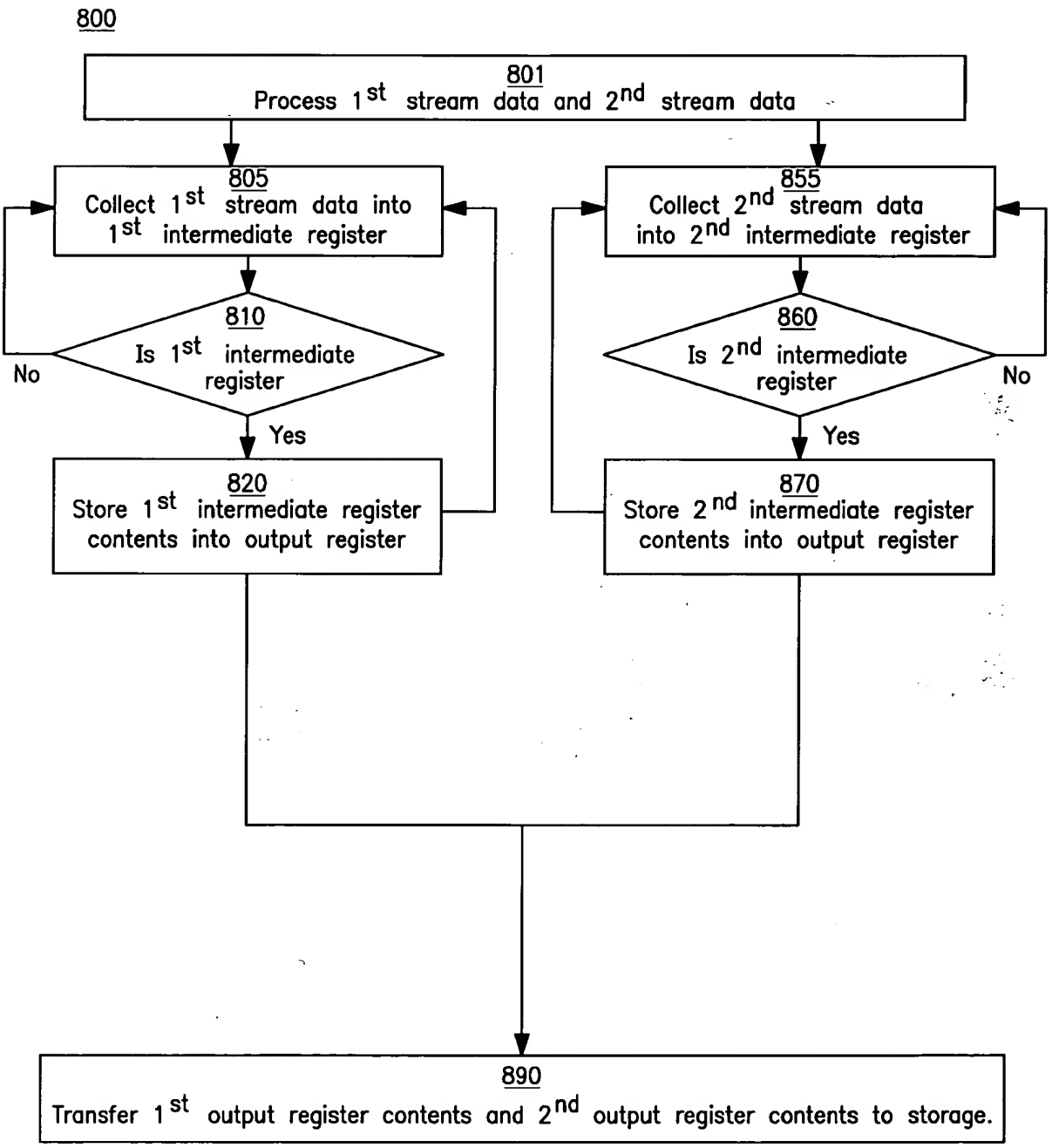
800
801
Process 1st stream data and 2nd stream data
805
Collect 1st stream data into 1st intermediate register
810
Is 1st intermediate register
No
Yes
820
Store 1st intermediate register contents into output register
855
Collect 2nd stream data into 2nd intermediate register
860
Is 2nd intermediate register
No
Yes
870
Store 2nd intermediate register contents into output register
890
Transfer 1st output register contents and 2nd output register contents to storage.

FIG. 8